Field-programmable Gate Array Implementation of Low-density Parity-check Codes Decoder and Hardware Testbed

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***Abstract* — The prototyping design of the channel coding in communication systems such as IEEE 802.16e (WiMAX) has become more sophisticated because of the increasing need for interoperability. Understanding its performance in the design and implementation of forward error correction codes in a real-time manner is necessary for rapid prototyping in research areas that are primarily based on emulation and stand-alone tests. This paper presents the design, implementation, experimental verification, and validation of the proposed LDPC decoder using a real-time FPGA based baseband test. The design of the LDPC decoder is described. In addition, a description of the hardware components that covers the important parts of the system from RF to channel decoding is included. The overall architecture of the baseband digital signal processing is simply illustrated, and details of the data acquisition module are provided. On the implementation and testing results, the throughput and latency at all the code rates specified in IEEE 802.16e are shown. Furthermore, the results for the architectural complexity and performance in terms of the bit error rates over the testbed show that the proposed flexible design for IEEE 802.16e exhibits potential under a practical environment.**

I. INTRODUCTION

Channel coding is a crucial component for next-generation wireless communications to enable high capacity and range. Recommendations on the classes of codes, including the parity-check matrices, coding rate, and data block length, can be easily found in standards suiting the designer's applications. A class of Low-Density Parity-Check codes (LDPC) [1] has been widely adopted as promising error correction codes because of their high performance in terms of the bit-error rate (BER) and design flexibility, which make them suitable for various applications. LDPC codes have been implemented in several standards. In the case of implementation, because code design and construction are recommended by the standards, efforts have been made toward architecture development and implementation techniques. Because LDPC encoder implementation presents less of a challenge, in the literature, several methods that focus on the implementation of an LDPC decoder have been reported [2]–[6]. A challenge arises because the parity-check matrix H of each code rate in the standards uses a large amount of memory, which complicates the hardware realization. Designing the optimal decoder requires a trade-off, primarily among the hardware complexity, throughput, and performance over a broadly used prototyping platform called a field-programmable gate array (FPGA).

However, the design of implementation architecture for such a code requires insight into its real-time system-level behavior, which emulates a real scenario. Normally in industrial research and development (R&D), most communication engineers employ a modern FPGA chip as a platform during the prototyping steps. In academic areas, the need for very-large-scale integration (VLSI) circuits has increased to some extent because there is a need to measure the designed circuits on interoperability issues to ensure that the proposed ideas meet the requirements of standards such as IEEE 802.11n. Therefore, testbeds based on a dedicated FPGA platform are playing important roles in both company and university laboratories.

The implementation of LDPC decoders in a real-time environment has received special attention from the research community. In [7], the implementation of a 4 × 4 multiple-input multiple-output (MIMO)-orthogonal frequency-division multiplexing (OFDM) transceiver on FPGA was presented, which also enabled the real-time testing of the channel coding. A testbed requires a large investment, making it infeasible for academic research that is not funded by the industrial sector. Thus, in this paper, we also present a method for setting up a real-time testbed platform to test our LDPC decoder.

This paper is organized as follows. In Section II, we describe implementation of the proposed LDPC decoder. The wireless testbed platform is illustrated and detailed in Section III. In Section IV, implementation results are presented and discussed. Finally, conclusions are drawn in Section V.

II. IMPLEMENTATION OF LDPC DECODER

To address the high demand for broadband wireless applications, a decoder design based on the block-circulant property was developed. This report presents an implementation of the LDPC decoder, which is able to decode all the code rates defined in IEEE 802.16e. It provides low area consumption and high performance for IEEE 802.16e applications and data storage systems such as hard disks.

The flexible LDPC decoder was designed by collecting the permutation numbers of the IEEE802.16e standard [8] in variable node processor (VNPs). We designed 24 VPNs and a single check node processor (CNP) according to IEEE 802.16e supporting every code rate. The channel latency has a range of 0.08–0.24 ms. The maximum throughput has a range of 9.6–27.91 Mbps. Gate cell arrays are used for the slice register, lookup table (LUT), and block RAM, which have values of 3086, 13555, and 15, respectively.

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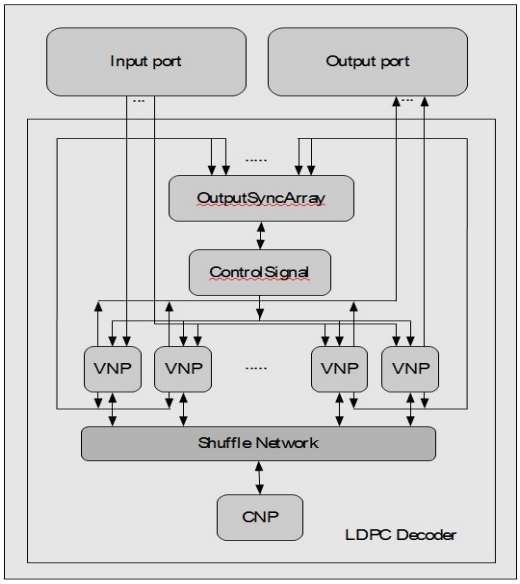

Fig. 1. Architecture of flexible LDPC decoder

In this study, the flexible LDPC decoder supported a code rate of 2304 bits and used the λ-min decoding algorithm for the benefit of using FPGA to implementation.

The architecture was constructed to reach the optimum number of used gate cells, throughput, and hardware resource limitations on an FPGA, Xilinx's Virtex-5. The ModelSim PE student edition program and Xilinx ISE were used for the simulation. When the simulation results were close to the company specifications, a prototype was constructed and tested to measure the specifications, which have already been presented in this report.

The architecture of LDPC decoder is shown in *Fig. 1*. Two interesting modules, ControlSignal unit and Output-SyncArray, are worth mentioned here. The ControlSignal consists of the control signal unit and ROM. ControlSignal is used to control status of VNPs and shuffle network according to the parity check matrix stored in ROM which is accessed by address bus. OutputSyncArray module makes sure that the processing in VNPs is completed and ready to send their output massages.

III. Wireless Testbed Platform

The main objective of the testbed is to construct a real-time in laboratory environment for channel code testing. As depicted in *Fig. 2,* our testbed comprises a signal source, 6-dB attenuators, noise source, RF combiner, A/D board, FPGA board, and computer for system controls and monitoring. First, an Agilent model E4438C 250 kHz–6 GHz vector signal generator (VSG) was employed as the signal source. After a reference signal is generated and outputs from the baseband studio digital signal interface module in the vector signal generator, it will be fed to the attenuator to reduce its strength, making it suitable for baseband processing in the A/D board, which is an AD9432 evaluation board from Analog Devices. An arbitrary waveform generator (AWG) was employed as the noise source, generating Gaussian noise which is fed to the combiner to superimpose it on the signal. Additionally, the IP core encoder/decoder LDPC code resides inside an FPGA board, which is a Xilinx ML501 with a Xilinx XC5VLX50 FPGA chip. The platform is described in the following subsections.

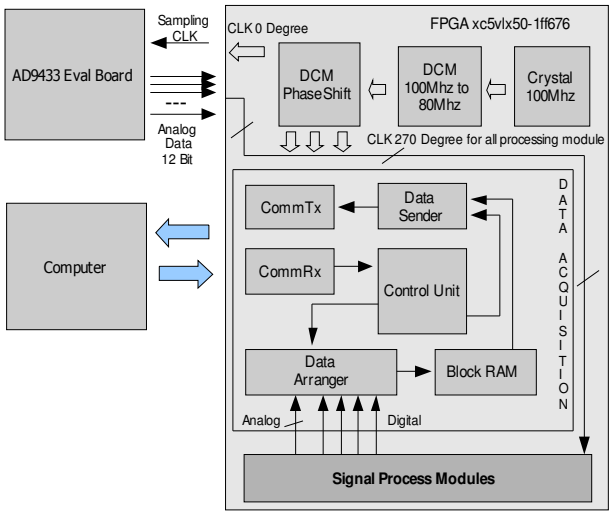

Fig. 3. Architecture overview of digital signal processing platform

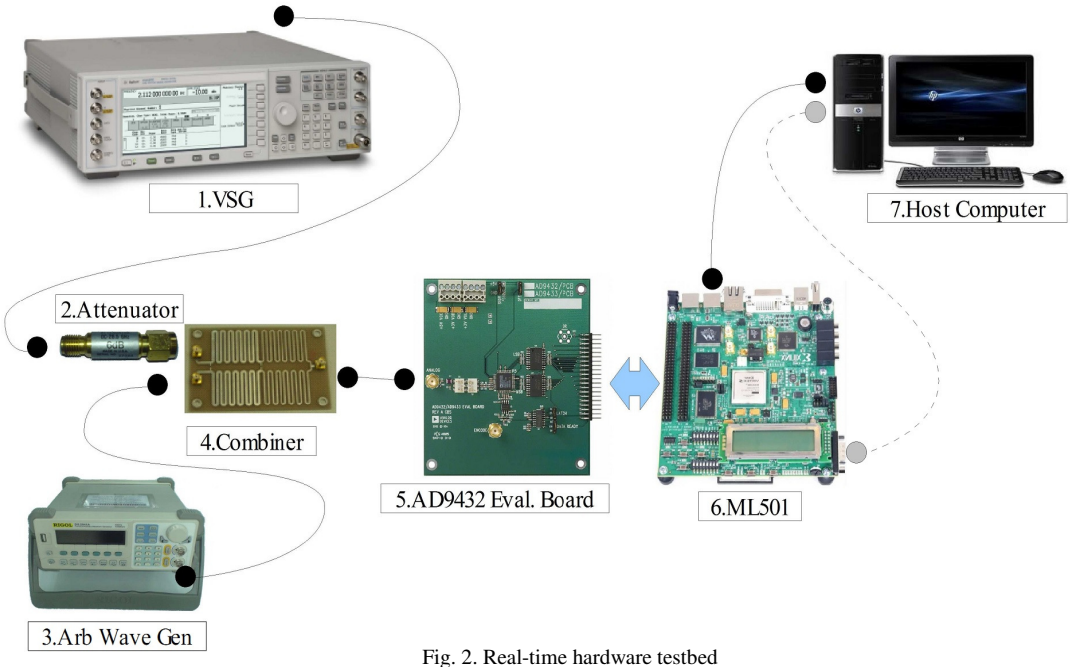

Fig. 2. Real-time hardware testbed

A. Analog RF Front end

The baseband signal is generated from VSG, where binary phase shift keying (BPSK) modulation is adopted to operate at 20 Mbps as Table I. The signal waveform, where "0"and "1" represent +0.5 and -0.5 volts, respectively, outputs Port I_OUT, which matches a 50-Ω impedance.

TABLE I: CONFIGURATION OF THE SET UP

Signal Waveform	Modulation Type	Symbol Rate
Baseband	BPSK	20 MS/s

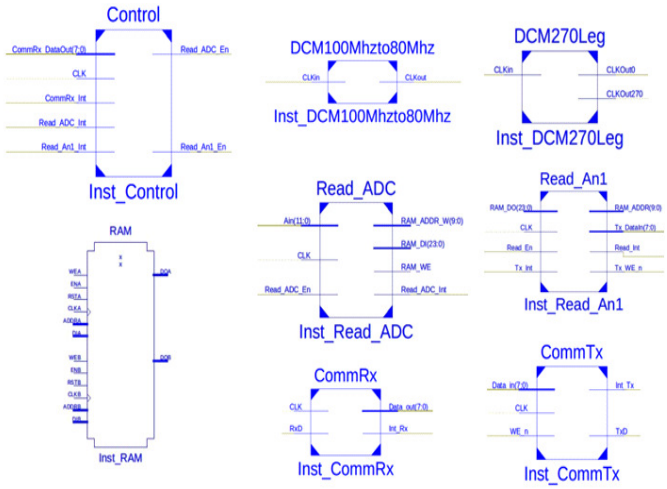

Fig. 4. Data acquisition components

B. Data Acquisition module

The data acquisition module in *Fig. 3,* communicates at baud rate 115.2 kbps. Sampling bits is 12 per symbol and signals are sampled 2048 symbols per instruction cycle. The module consists of several subcomponents as illustrated in *Fig. 4.* It is worth mentioned that the instruction for storing and returning the data is 0x41. The module is operated at a clock speed of 80 MHz. The board requires power supply of +5 V and +3 V while power supply of-5V is not necessary. After data acquisition module, digital data sequence is transmitted from AD9433 board via PIN header with 2.54 mm size as same as the FPGA ML501 board. AD9432 which is an AC coupled device can be operated at 10 Mbps without problems on connection.

IV. IMPLEMENTATION RESULTS

The proposed LDPC decoder design focuses on primary criteria that include the area, throughput, latency, and BER performance, whereas other criteria such as the energy dissipation and error floor are not considered here. The measurement was accomplished over the previously mentioned testbed.

From the Table II, it can be seen that almost throughput and latency were performed for LDPC codes specified in IEEE 802.16e with 10 iterations and the decoding clock frequency of 100 MHz, the maximum throughput of 27.91 Mbps and lantency of 0.08 ms.

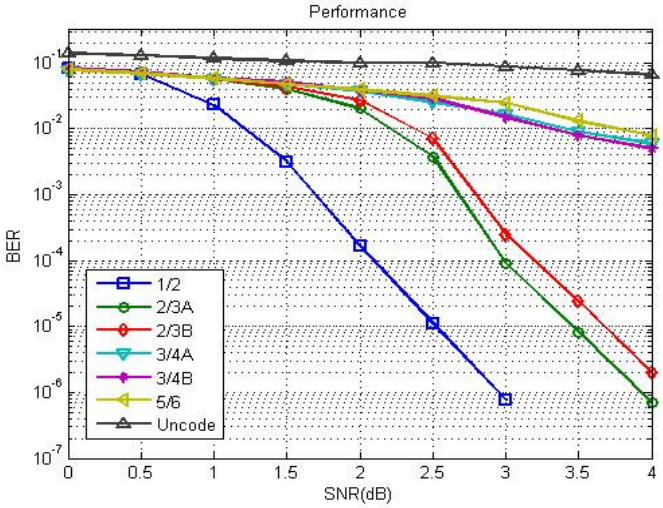

Fig. 5. BER performance of the decoder

TABLE II. THROUGHPUT AND LATENCY

Code Rate	Throughput (Mbps)	Latency (ms)
1/2	9.60	0.24
2/3A	14.03	0.16
2/3B	14.03	0.16
3/4A	18.89	0.12
3/4B	18.89	0.12
5/6	27.91	0.08

TABLE III. SYNTHESIS RESULTS OF LDPC DECODER FOR IEEE 802.16E ON XC5VLX50

Slice Logic Utilization	Used	Available	Utilization
Number of Slice Registers	3,086	28,800	10%
Number of Slice LUTs	13,555	28,800	47%
Number of Block RAM	15	48	31%
Number of occupied Slices	4,446	7,200	61%
Number of fully used LUT Flip Flop pairs	3,068	13,573	22%
Number of bonded IOBs	148	440	33%

Table III shows the area complexity synthesized for the Xilinx XC5VLX50 model FPGA with multi-rate LDPC cores at a fixed block length of 2304 bits. Table III summarizes the slice LUTs, occupied slice, and LUT flip-flop pairs utilized for the LDPC decoder design.

In order to verify the performance of each code rate, various tests were conducted over the baseband platform, as depicted in *Fig. 5.*

V. CONCLUSIONS

The design, implementation and testing of the proposed flexible LDPC decoder for IEEE 802.16e standard over the real-time testbed has been described and discussed. The design of the LDPC decoder facilitates the block circulant property to achieving better trade-off between implementation area and throughput. The architecture of the testbed

promisingly enables integration tests to academic research without investment on specialized intellectual properties on software stack and soft cores. To explore tradeoff among throughput, implementation areas, and performance the throughput and the latency at all code rates specified in IEEE 802.16e, the architectural complexity, and bit error rates over the testbed were measured. From those results, the proposed flexible design for IEEE 802.16e exhibits potentials under practical environment.

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